400G QSFP-DD-to-4×100G QSFP56 Breakout Active Optical Cable

Key Features

- ❑ Low latency DSP-free electronics-based CDR
- ❑ Multi-data rate up to 56.15 Gb/s per lane
- ❑ PAM4 modulation
- ❑ Single 3.3 V power supply
- ❑ Low power consumption : 7.6 W on 400G end, 2.3 W on 100G end with all CDRs enabled
- ❑ Up to 100 m length
- ❑ QSFP-DD MSA compliant
- ❑ CMIS 3.0/4.0 compliant
- ❑ Commercial operating case temperature range: 0 to 70˚C
- ❑ Hot pluggable
- ❑ RoHS/REACH compliant
- ❑ TUV-certified
- ❑ LSZH, LSZH/OFNR or OFNP-rated cable

Applications

- ❑ IEEE 802.3cm 400GBASE SR8
- ❑ Datacenter: servers, switches, storages and NIC adapters
- ❑ Proprietary HPC interconnections

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1. Absolute Maximum Ratings

Parameters	Symbol	Min.	Typ.	Max.	Unit	Note
Supply Voltage	V_{IN}	0	-	4.0	V	
Input Swing	V_{IN-MAX}			1500	mVpp	
Storage Temperature	T_{STG}	-40	-	85	˚C	Ambient
Relative Humidity	RH	5	-	85	%	

2. Operating Specifications

Parameters		Symbol	Min.	Typ.	Max.	Unit	Note
Operating Case Temperature		T_{OP}	0	-	70	˚C	
Power Supply Voltage		V_{CC}	3.15	3.30	3.47	V	
Power Supply Current	400G End	I_{CC}	-	2300	2500	mA	1
	100G End		-	680	750	mA	
Power Consumption	400G End	P	-	7.6	8.0	W	1
	100G End		-	2.3	2.5	W	

3. Electrical Characteristics

Parameters	Symbol	Min.	Typ.	Max.	Unit	Note
Data Rate (Per Channel)	BR	-	26.5625	-	GBd	2
Transmitter						
Input Differential Impedance	R_{IN}	90	100	110	Ω	
Differential Data Input Voltage	V_{INP-P}	900			mV	
Receiver						
Output Differential Impedance	R_{OUT}	90	100	110	Ω	
Differential Data Output Voltage	V_{OUTP-P}	-	800	-	mV	
Bit Error Ratio (at 26.5625 GBd)	-	-	-	2.4×10^{-4}	-	3

Note:
1. Per end, all channel CDRs are enabled.
2. Dual data rate of 25.78125 and 28.07618 Gbaud are available upon request.
3. Pre-FEC Bit Error Ratio with a PRBS $2^{31}-1$ test pattern over a normal operating temperature range.

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4. Pin Description (400G QSFP-DD End)

Pin	Logic	Name	Description	Note
1		GND	Ground	1
2	CML-I	Tx2n	Transmitter Inverted Data Input	
3	CML-I	Tx2p	Transmitter Non-Inverted Data Input	
4		GND	Ground	1
5	CML-I	Tx4n	Transmitter Inverted Data Input	
6	CML-I	Tx4p	Transmitter Non-Inverted Data Input	
7		GND	Ground	1
8	LVTTL-I	ModSelL	Module Select	
9	LVTTL-I	ResetL	Module Reset	
10		VccRx	+3.3V Power Supply Receiver	2
11	LVCMOS-I/O	SCL	2-wire Serial Interface Clock	
12	LVCMOS-I/O	SDA	2-wire Serial Interface Data	
13		GND	Ground	1
14	CML-O	Rx3p	Receiver Non-Inverted Data Output	
15	CML-O	Rx3n	Receiver Inverted Data Output	
16		GND	Ground	1
17	CML-O	Rx1p	Receiver Non-Inverted Data Output	
18	CML-O	Rx1n	Receiver Inverted Data Output	
19		GND	Ground	1
20		GND	Ground	1
21	CML-O	Rx2n	Receiver Inverted Data Output	
22	CML-O	Rx2p	Receiver Non-Inverted Data Output	
23		GND	Ground	1
24	CML-O	Rx4n	Receiver Inverted Data Output	
25	CML-O	Rx4p	Receiver Non-Inverted Data Output	
26		GND	Ground	1
27	LVTTL-O	ModPrsL	Module Present	
28	LVTTL-O	IntL	Interrupt	
29		VccTx	+3.3V Power Supply Transmitter	2
30		Vcc1	+3.3V Power Supply	2
31	LVTTL-I	InitMode	Initialization Mode; In legacy QSFP applications, LPMode	
32		GND	Ground	1
33	CML-I	Tx3p	Transmitter Non-Inverted Data Input	
34	CML-I	Tx3n	Transmitter Inverted Data Input	
35		GND	Ground	1
36	CML-I	Tx1p	Transmitter Non-Inverted Data Input	
37	CML-I	Tx1n	Transmitter Inverted Data Input	
38		GND	Ground	1

Note:

1. GND is the symbol for signal and supply (power) common for the QSFP-DD module. All are common within the QSFP-DD module and all module voltages are referenced to this potential unless otherwise noted.
2. VccRx, VccRx1, Vcc1, Vcc2, VccTx and VccTx1 shall be applied concurrently. The connector pins are each rated for a maximum current of 1000 mA.
3. All Vendor Specific, Reserved, No Connect and ePPS pins may be terminated with 50 ohms to ground on the host, and not connected within the Module. Pad 65 (No Connect) is left unconnected within the module.

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4. Pin Description (400G QSFP-DD End)

Pin	Logic	Name	Description	Note
39		GND	Ground	1
40	CML-I	Tx6n	Transmitter Inverted Data Input	
41	CML-I	Tx6p	Transmitter Non-Inverted Data Input	
42		GND	Ground	1
43	CML-I	Tx8n	Transmitter Inverted Data Input	
44	CML-I	Tx8p	Transmitter Non-Inverted Data Input	
45		GND	Ground	1
46		Reserved	For future use	3
47		VS1	Module Vendor Specific 1	3
48		VccRx1	3.3V Power supply	2
49		VS2	Module Vendor Specific 2	3
50		VS3	Module Vendor Specific 3	3
51		GND	Ground	1
52	CML-O	Rx7p	Receiver Non-Inverted Data Output	
53	CML-O	Rx7n	Receiver Inverted Data Output	
54		GND	Ground	1
55	CML-O	Rx5p	Receiver Non-Inverted Data Output	
56	CML-O	Rx5n	Receiver Inverted Data Output	
57		GND	Ground	1
58		GND	Ground	1
59	CML-O	Rx6n	Receiver Inverted Data Output	
60	CML-O	Rx6p	Receiver Non-Inverted Data Output	
61		GND	Ground	1
62	CML-O	Rx8n	Receiver Inverted Data Output	
63	CML-O	Rx8p	Receiver Non-Inverted Data Output	
64		GND	Ground	1
65		NC	No Connect	3
66		Reserved	For future use	3
67		VccTx1	3.3V Power Supply	2
68		Vcc2	3.3V Power Supply	2
69	LVTTL-I	ePPS	Precision Time Protocol (PTP) refence clock input	3
70		GND	Ground	1
71	CML-I	Tx7p	Transmitter Non-Inverted Data Input	
72	CML-I	Tx7n	Transmitter Inverted Data Input	
73		GND	Ground	1
74	CML-I	Tx5p	Transmitter Non-Inverted Data Input	
75	CML-I	Tx5n	Transmitter Inverted Data Input	
76		GND	Ground	1

Note:

1. GND is the symbol for signal and supply (power) common for the QSFP-DD module. All are common within the QSFP-DD module and all module voltages are referenced to this potential unless otherwise noted.
2. VccRx, VccRx1, Vcc1, Vcc2, VccTx and VccTx1 shall be applied concurrently. The connector pins are each rated for a maximum current of 1000 mA.
3. All Vendor Specific, Reserved, No Connect and ePPS pins may be terminated with 50 ohms to ground on the host, and not connected within the Module. Pad 65 (No Connect) is left unconnected within the module.

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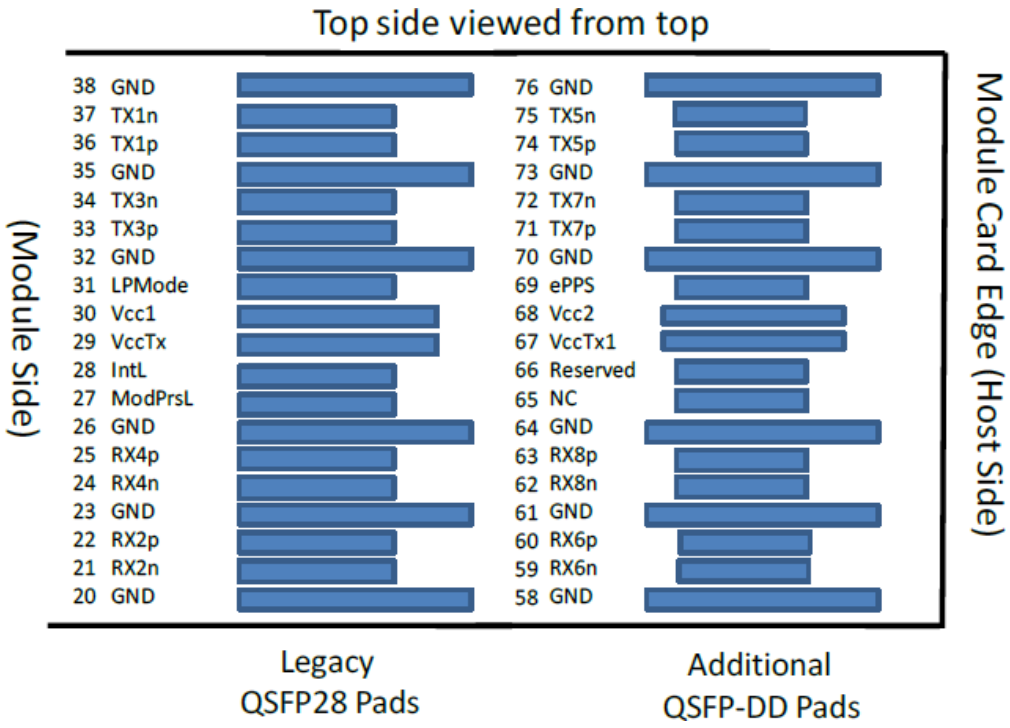
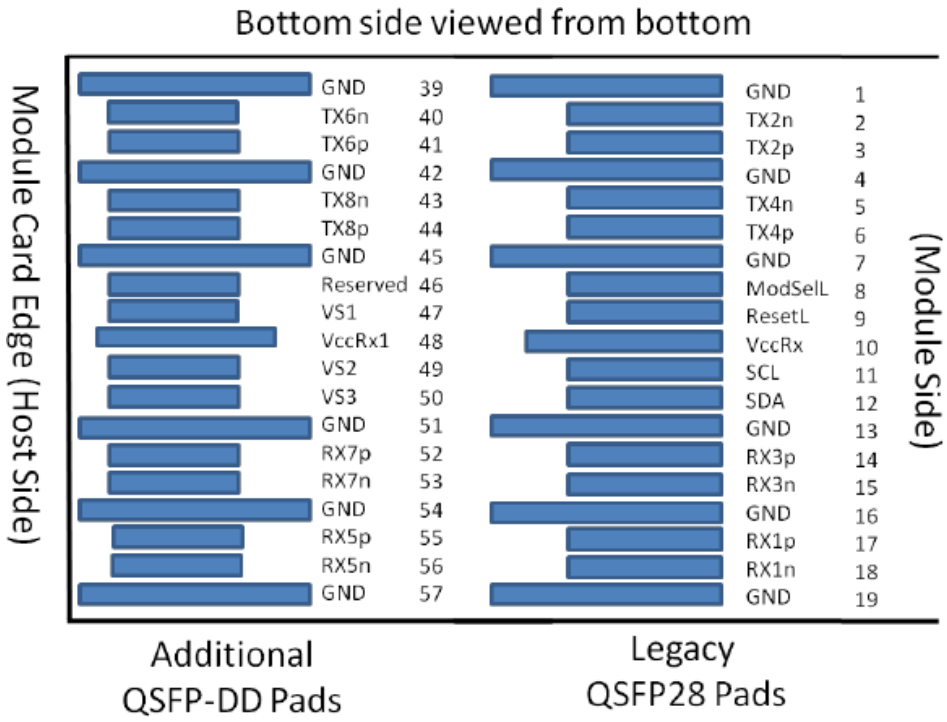
4. Pin Description (400G QSFP-DD End)





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4. Pin Description (100G QSFP56 End)

Pin	Logic	Name	Description	Note
1		GND	Ground	1
2	CML-I	Tx2n	Transmitter Inverted Data Input	
3	CML-I	Tx2p	Transmitter Non-Inverted Data Input	
4		GND	Ground	1
5	CML-I	Tx4n	Transmitter Inverted Data Input	3
6	CML-I	Tx4p	Transmitter Non-Inverted Data Input	3
7		GND	Ground	1
8	LVTTL-I	ModSelL	Module Select	
9	LVTTL-I	ResetL	Module Reset	
10		Vcc Rx	+3.3V Power supply receiver	2
11	LVCMOS-I/O	SCL	2-wire serial interface clock	
12	LVCMOS-I/O	SDA	2-wire serial interface data	
13		GND	Ground	1
14	CML-O	Rx3p	Receiver Non-Inverted Data Output	3
15	CML-O	Rx3n	Receiver Inverted Data Output	3
16		GND	Ground	1
17	CML-O	Rx1p	Receiver Non-Inverted Data Output	
18	CML-O	Rx1n	Receiver Inverted Data Output	
19		GND	Ground	1
20		GND	Ground	1
21	CML-O	Rx2n	Receiver Inverted Data Output	
22	CML-O	Rx2p	Receiver Non-Inverted Data Output	
23		GND	Ground	1
24	CML-O	Rx4n	Receiver Inverted Data Output	3
25	CML-O	Rx4p	Receiver Non-Inverted Data Output	3
26		GND	Ground	1
27	LVTTL-O	ModPrsL	Module Present	
28	LVTTL-O	IntL	Interrupt	
29		Vcc Tx	+3.3V Power supply transmitter	2
30		Vcc 1	+3.3V Power Supply	2
31	LVTTL-I	LPMode	Low Power Mode	
32		GND	Ground	1
33	CML-I	Tx3p	Transmitter Non-Inverted Data Input	3
34	CML-I	Tx3n	Transmitter Inverted Data Input	3
35		GND	Ground	1
36	CML-I	Tx1p	Transmitter Non-Inverted Data Input	
37	CML-I	Tx1n	Transmitter Inverted Data Input	
38		GND	Ground	1

Note

1. GND is the symbol for signal and supply (power) common for the QSFP module. All are common within the QSFP module and all module voltages are referenced to this potential unless otherwise noted. Connect these directly to the host board signal-common ground plane.
2. Vcc Rx, Vcc1 and Vcc Tx are the receiver and transmitter power supplies and shall be applied concurrently. Vcc Rx, Vcc1 and Vcc Tx may be internally connected within the QSFP transceiver module in any combination. The connector pins are each rated for a maximum current of 500 mA.
3. Not used

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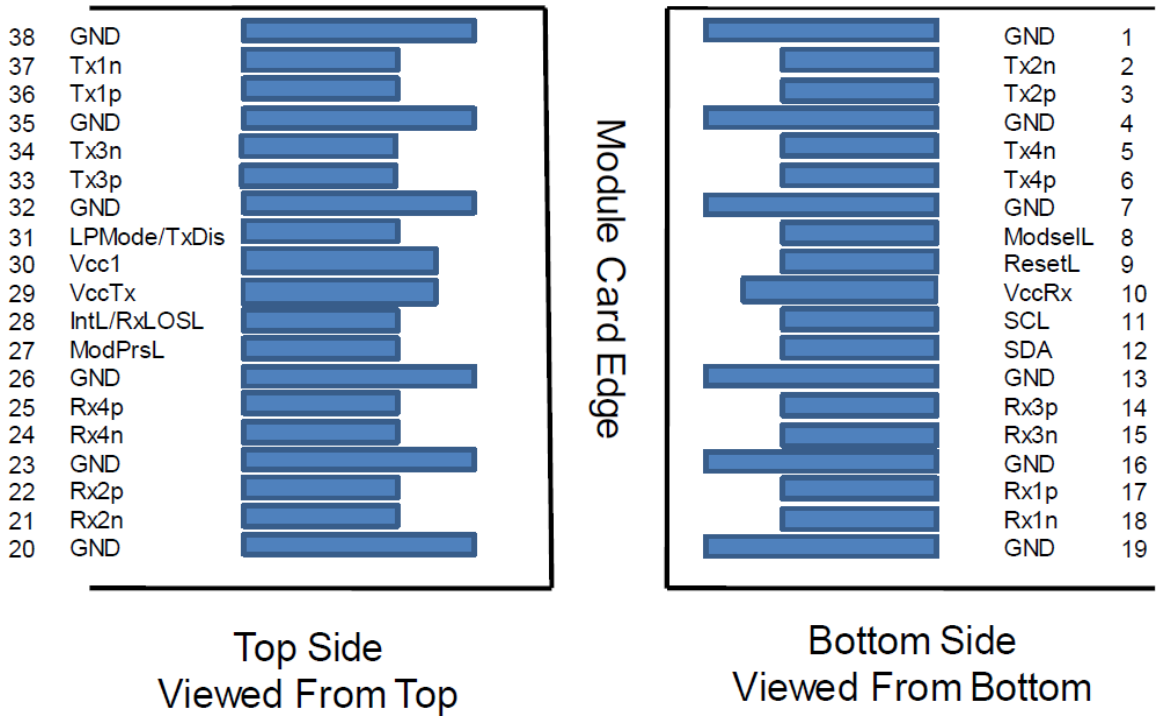
4. Pin Description (100G QSFP56 End)



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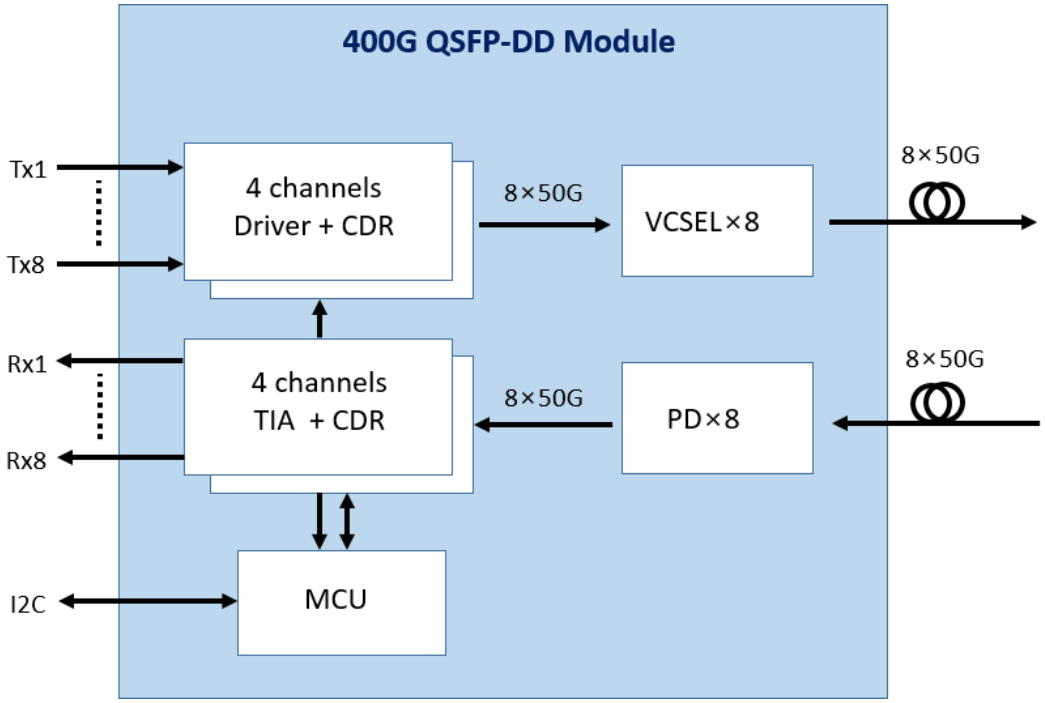
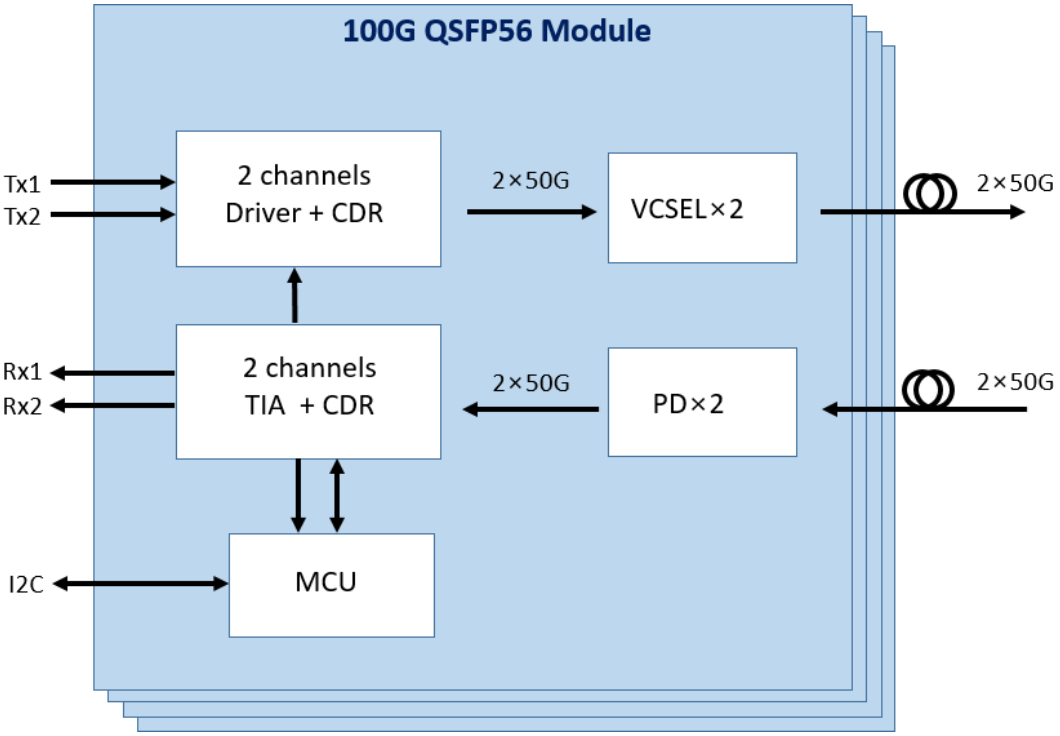
5. Block Diagram





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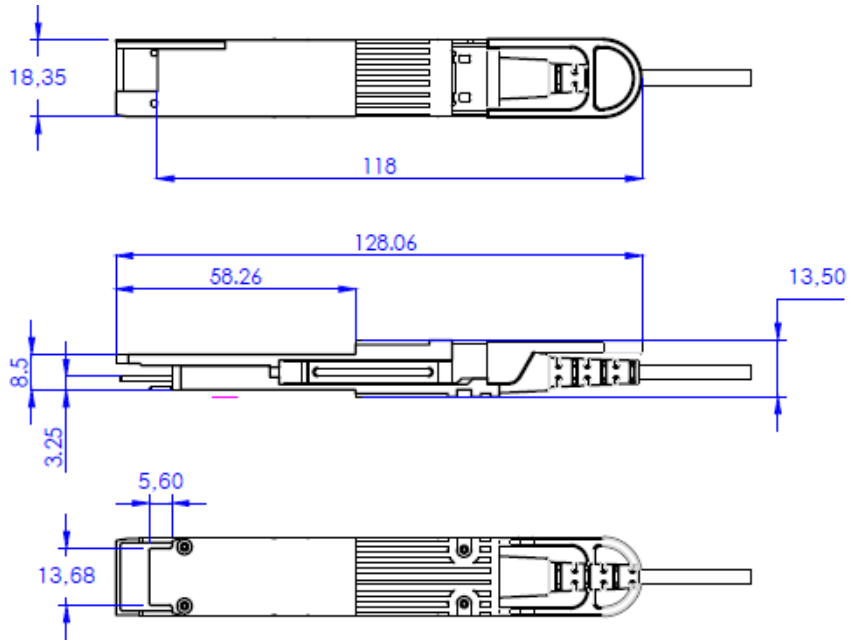
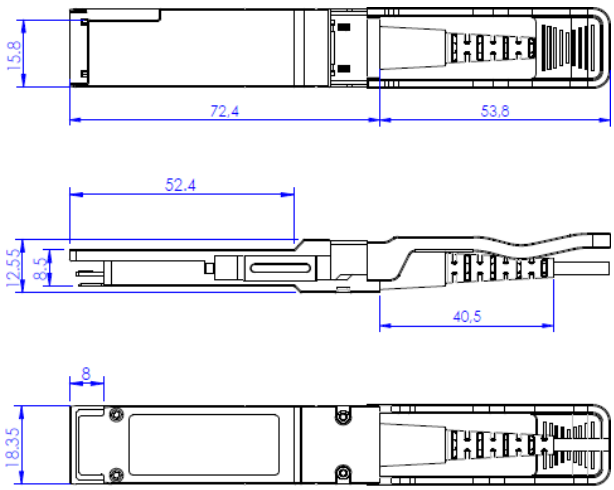
6. Mechanical Specifications

Unit: mm



400G QSFP-DD End



100G QSFP56 End

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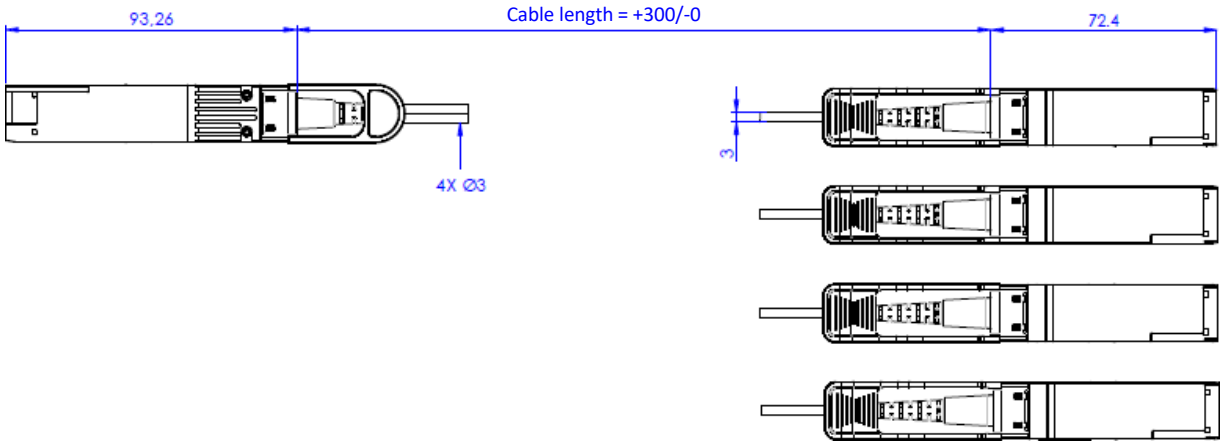
6. Mechanical Specifications

Unit: mm



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7. Active Optical Cable

Parameters	Value	Unit	Note
Cable Diameter	• LSZH, LSZH/OFNR: Ø3.0 ± 0.15 • OFNP: Ø3.0 ± 0.20	mm	
Minimum Bend Radius	30	mm	Without tension
	60	mm	Under maximum tension
Length Tolerance	+300 / -0	mm	
Cable Jacket	LSZH, LSZH/OFNR or OFNP-rated, Aqua		

8. Ordering Information

Part Number	Description	Note
MD400FOEXXyyyZZ	QSFP-DD-to-4×QSFP56, AOC, Ethernet, yyy m, three-digit number yyy for length in meter	
MD400FOIXXyyyZZ	QSFP-DD-to-4×QSFP56, AOC, InfiniBand, yyy m, three-digit number yyy for length in meter	

Note
1. Length (yyy)
   - The maximum cable length is 70 m with OM3 or 100 m with OM4.
   - The first digit A, B or C of the three-digit number denotes 0.25 m, 0.50 m and 0.75 m, respectively.
   - The first digit A, B or C of the three-digit number can be used for the cable length no greater than 10 m.
2. Cable jacket type (XX): GA (LSZH), GB (LSZH/OFNR), GC (OFNP)
3. Customer ID (ZZ): To be assigned upon request.

Examples

Part Number	Description
MD400FOEGAB00ZZ	400G QSFP-DD-to-4×100G QSFP56, AOC, Ethernet, LSZH, 0.5m
MD400FOIGBA09ZZ	400G QSFP-DD-to-4×100G QSFP56, AOC, InfiniBand, LSZH/OFNR, 9.25 m
MD400FOEGCC01ZZ	400G QSFP-DD-to-4×100G QSFP56, AOC, Ethernet, OFNP, 1.75 m

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9. Revision History

Version	Date	Description
1.0	Jun. 8, 2021	Initial release
1.01	Oct. 1, 2021	Added a detailed minimum bend radius value in Sec. 7

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